

INTEL(R) E7500 High Performance Appliance Platform
-Intel(R) XEON(TM) Processor or Low Voltage Intel (R)
XEON(TM) Processor with 512 KB L2 Cache

IO BOARD SCHEMATIC

PAGE	DESCRIPTION
1	CONTENT
2	REVISION CHANGES
3	BLOCK DIAGRAM
4	LAYOUT NOTICE
5	LAYOUT NOTICE
6	TABLES
7	P64H2#1 PCI-X BUS A,B
8	P64H2#1 HUB,POWER,GND
9	P64H2#1 TERMINATORS
10	P64H2#2 PCI-X BUS A,B
11	P64H2#2 HUB, POWER,GND
12	P64H2#2 TERMINATORS
13	P64H2#3 PCI-X BUS A,B
14	P64H2#3 HUB,POWER,GND
15	P64H2#3 TERMINATORS
16	GIGABIT/COPPER BUS INTERFACE
17	GIGABIT/COPPER POWER/GND/RJ45
18	GIGABIT FIBER1 PCI-X BUS INTERFACE
19	GIGABIT FIBER1 POWER/GND/SERDES

PAGE	DESCRIPTION
20	GIGABIT FIBER2 PCI-X BUS INTERFACE
21	GIGABIT FIBER 2 POWER/GND/SERDES
22	PCI-X SLOT
23	MICTOR HUB INTERFACE

THIS SCHEMATIC IS PROVIDED
"AS IS" WITH NO WARRANTIES
WHATSOEVER, INCLUDING ANY
WARRANTY OF
MERCHANTABILITY, FITNESS
FOR ANY PARTICULAR PURPOSE,
OR ANY WARRANT OTHERWISE
ARISING OUT OF PROPOSAL,
SPECIFICATION OR SAMPLE.

No license, express or implied, by
estoppel or otherwise, to any
intellectual property rights is granted
herein.

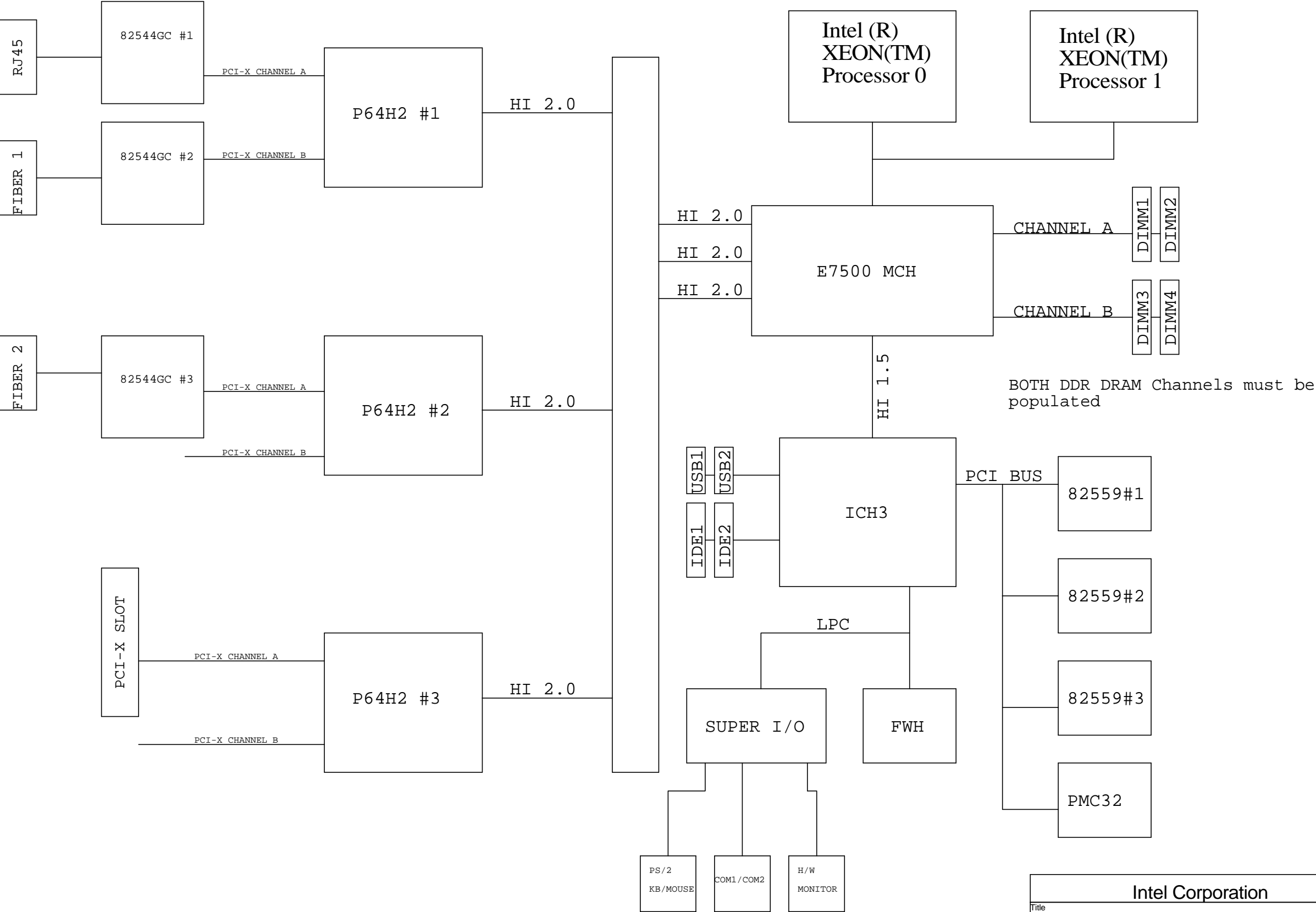
IO BOARD SCHEMATIC
rev 1.01

Intel Corporation		
Title IO BOARD		
Size	Document Number CONTENT	Rev 1.01
Date:	Monday, August 26, 2002	Sheet 1 of 23

IO BOARD SCHEMATIC rev 0.91 non NDA
IO BOARD SCHEMATIC rev 1.01 non NDA supporting
Intel(R) Xeon(TM) and Low Voltage Intel XEON(TM)
processors with 512 KB L2 Cache

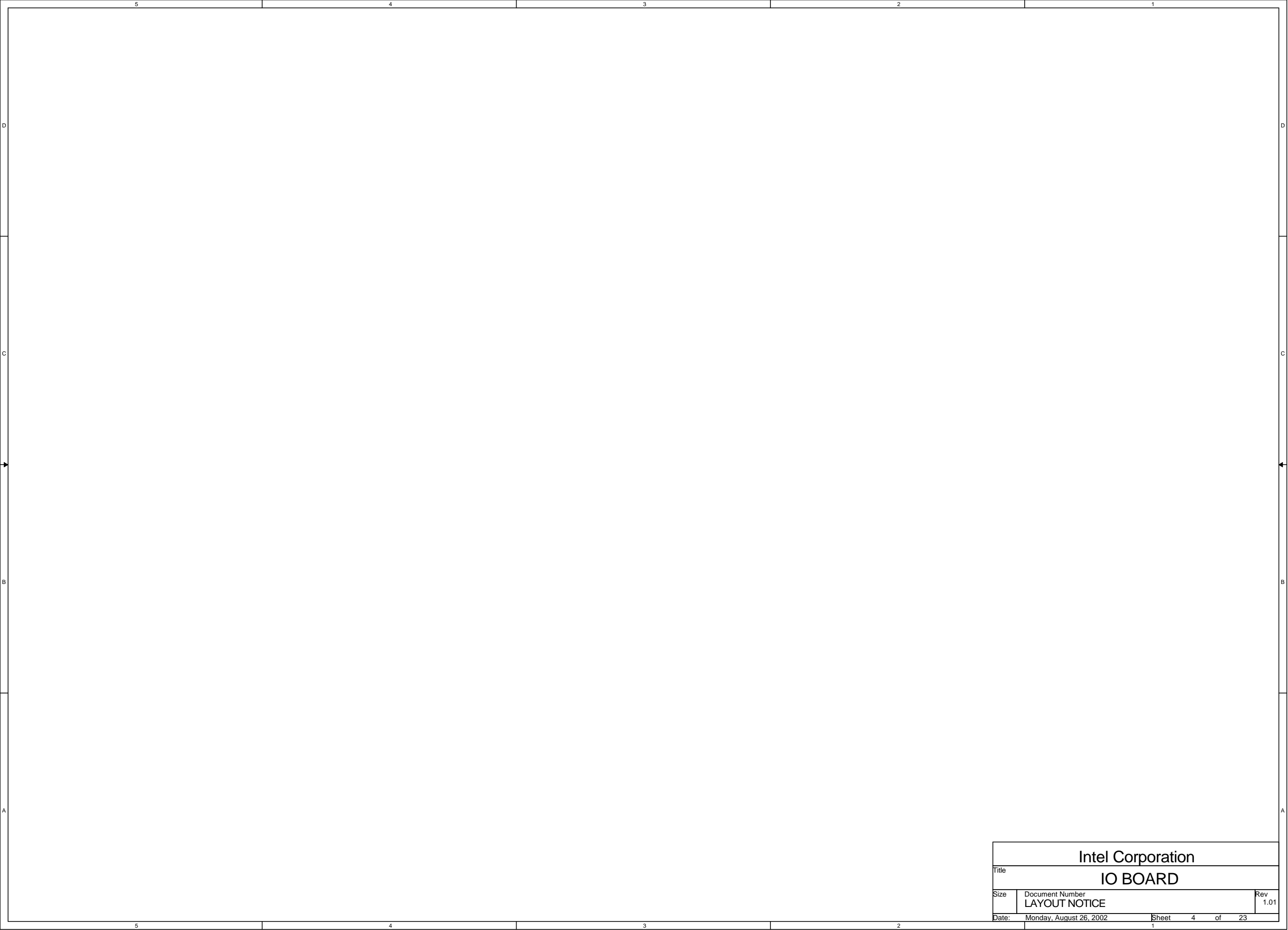
Intel Corporation			
Title IO BOARD			
Size	Document Number REVISION CHANGES		Rev 1.01
Date:	Monday, August 26, 2002	Sheet 2 of 23	1

INTEL(R) E7500 High Performance Appliance Platform Intel(R)
XEON(TM) Processor or Low Voltage Intel (R) XEON(TM) Processor with
512 KB L2 Cache

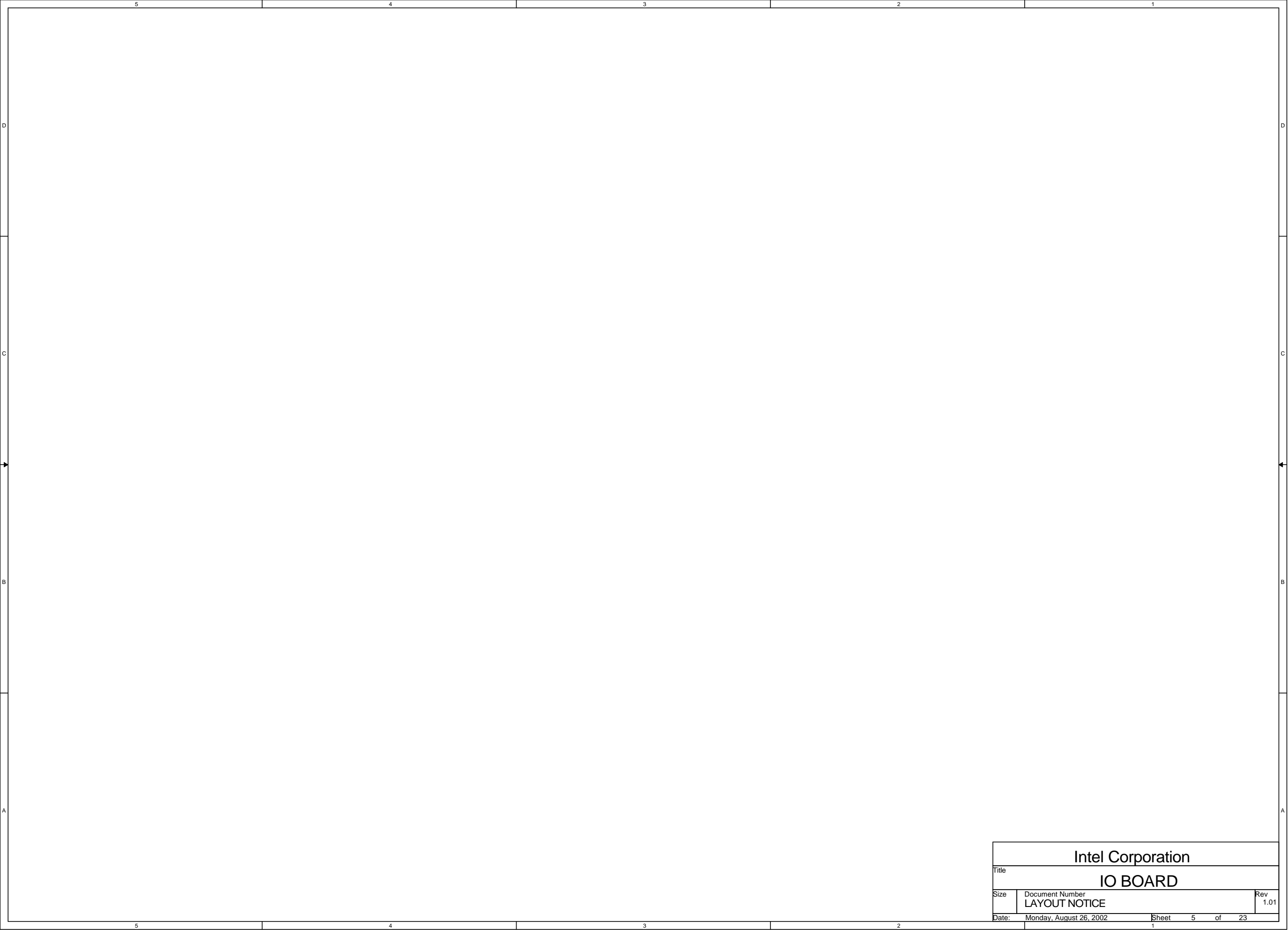


BOTH DDR DRAM Channels must be populated

Intel Corporation		
Title IO BOARD		
Size	Document Number BLOCK DIAGRAM	Rev 1.01
Date:	Monday, August 26, 2002	Sheet 3 of 23



Intel Corporation			
Title IO BOARD			
Size	Document Number LAYOUT NOTICE		Rev 1.01
Date:	Monday, August 26, 2002	Sheet 1	4 of 23



Intel Corporation			
Title IO BOARD			
Size	Document Number LAYOUT NOTICE		Rev 1.01
Date:	Monday, August 26, 2002	Sheet	5 of 23

CONNECTORS:

J1: ITP PORT
J2: COPPER GIGABIT PORT
J3: FIBER GIGABIT PORT
J4: FIBER GIGABIT PORT
J5: PCI-X SLOT
J6: USB PORT
J7: USB PORT
J8: RESET BUTTON
J9: COM1 PORT
J10: POWER BUTTON
J11: PS/2 KB/MOUSE
J12: 10/100M BITS RJ45
J13: 10/100M BITS RJ45
J14: 10/100M BITS RJ45
J15: LEDS CONNECTOR
IDE1: PRIMARY IDE CONNECTOR
IDE2: SECONDARY IDE CONNECTOR
ATX1: ATX POWER CONNECTOR
CPUFAN1: CPU FAN POWER CONNECTOR
CPUFAN2: CPU FAN POWER CONNECTOR

INTERRUPT ROUTING
TABLES:

ICH3 INTERRUPT:	P64H2#1
PIRQA#:	P64H2#1
PIRQB#:	P64H2#2
PIRQC#:	P64H2#3
PIRQD#:	NO USE
PIRQE#:	82559#1
PIRQF#:	82559#2
PIRQG#:	82559#3
PIRQH#:	NO USE

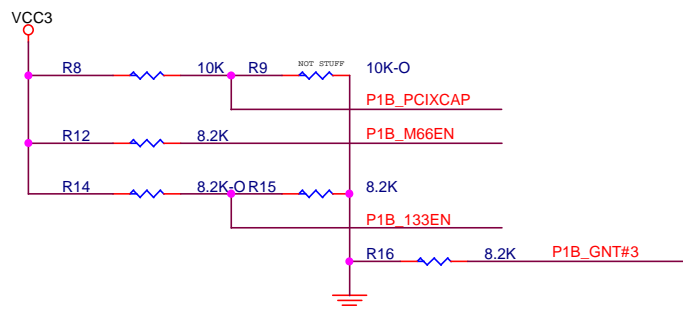
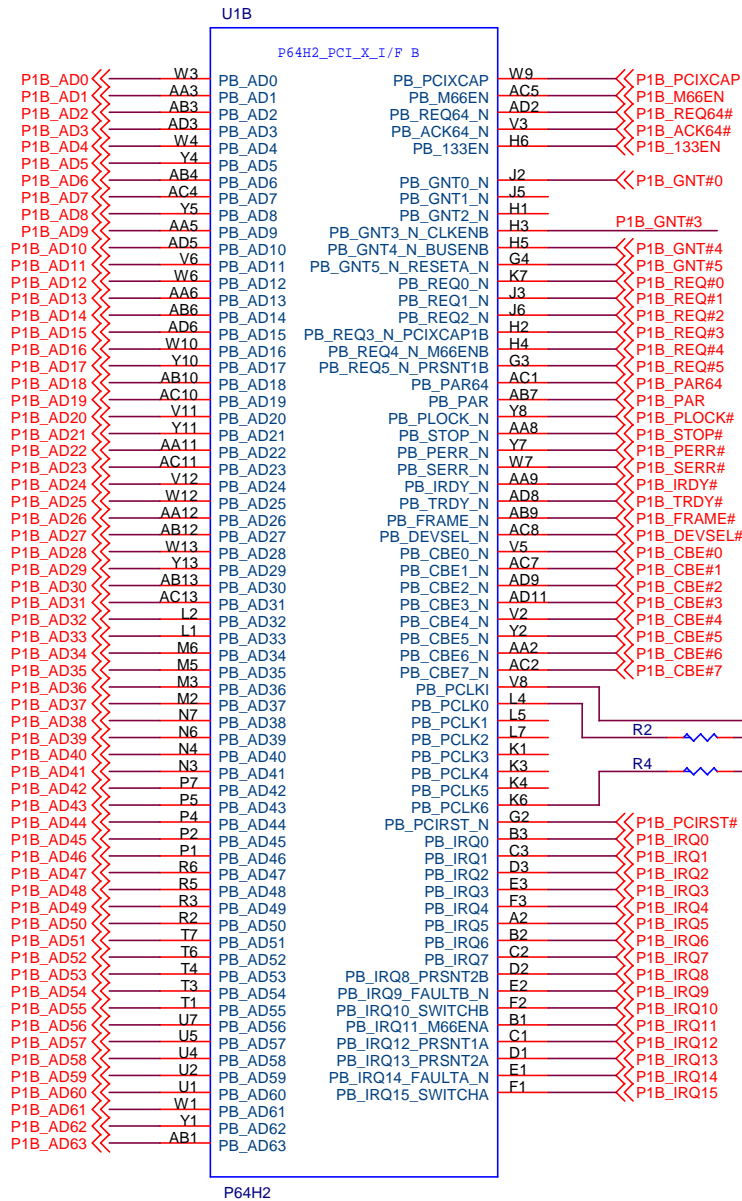
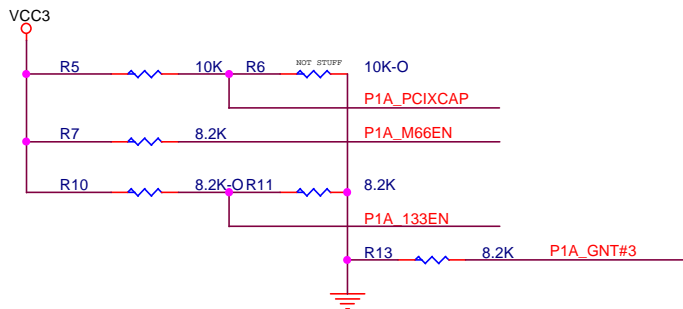
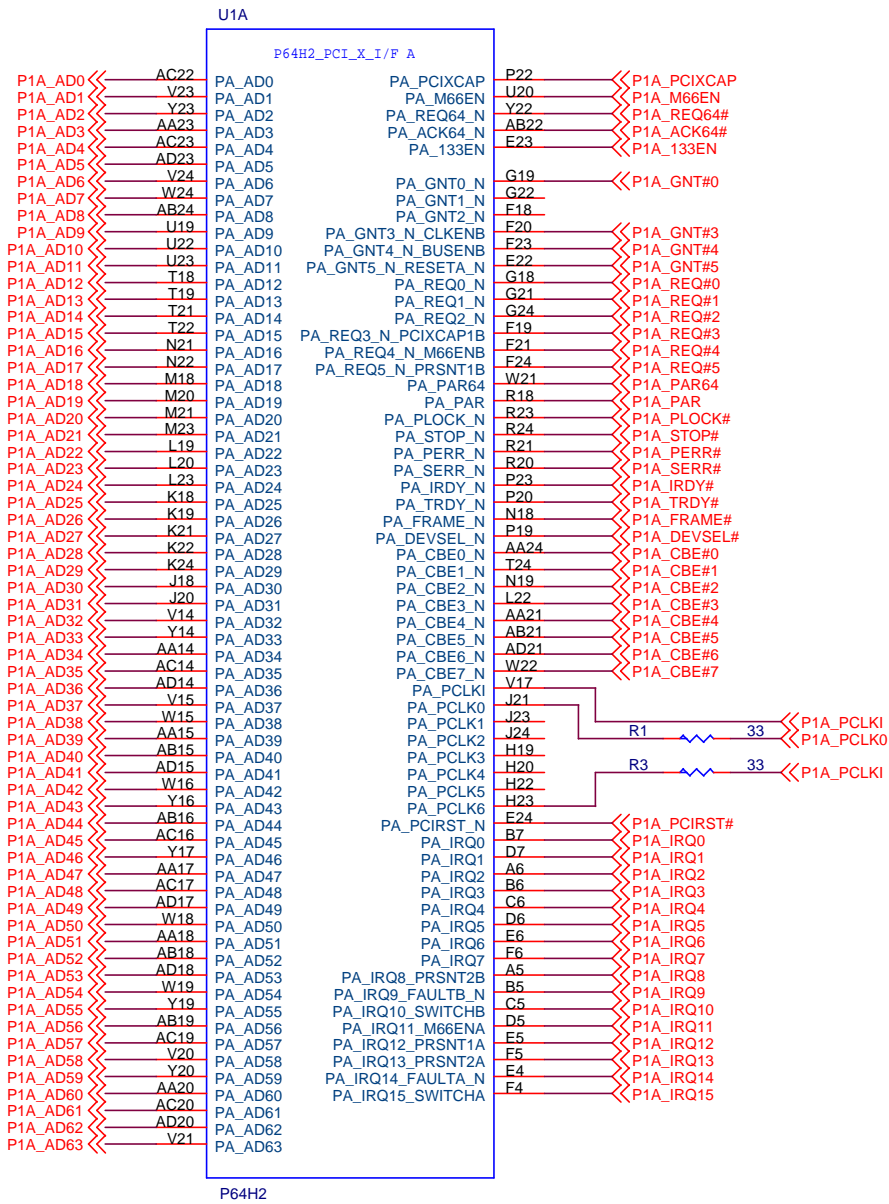
GPIO FOR LEDS

GPIO34: LED CONTROL FOR POWER LED
GPIO35: LED CONTROL FOR CPU OVER HEAT LED
GPIO36: LED CONTROL FOR PRIMARY HDD LED
GPIO37: LED CONTROL FOR SECONDARY HDD LED
GPIO38: LED CONTROL FOR 10/100M BIT PORT1 ACTIVITY LED
GPIO39: LED CONTROL FOR 10/100M BIT PORT2 ACTIVITY LED
GPIO40: LED CONTROL FOR 10/100M BIT PORT3 ACTIVITY LED
GPIO41: LED CONTROL FOR GIGABIT PORT1 ACTIVITY LED
GPIO42: LED CONTROL FOR GIGABIT PORT2 ACTIVITY LED
GPIO43: LED CONTROL FOR GIGABIT PORT3 ACTIVITY LED

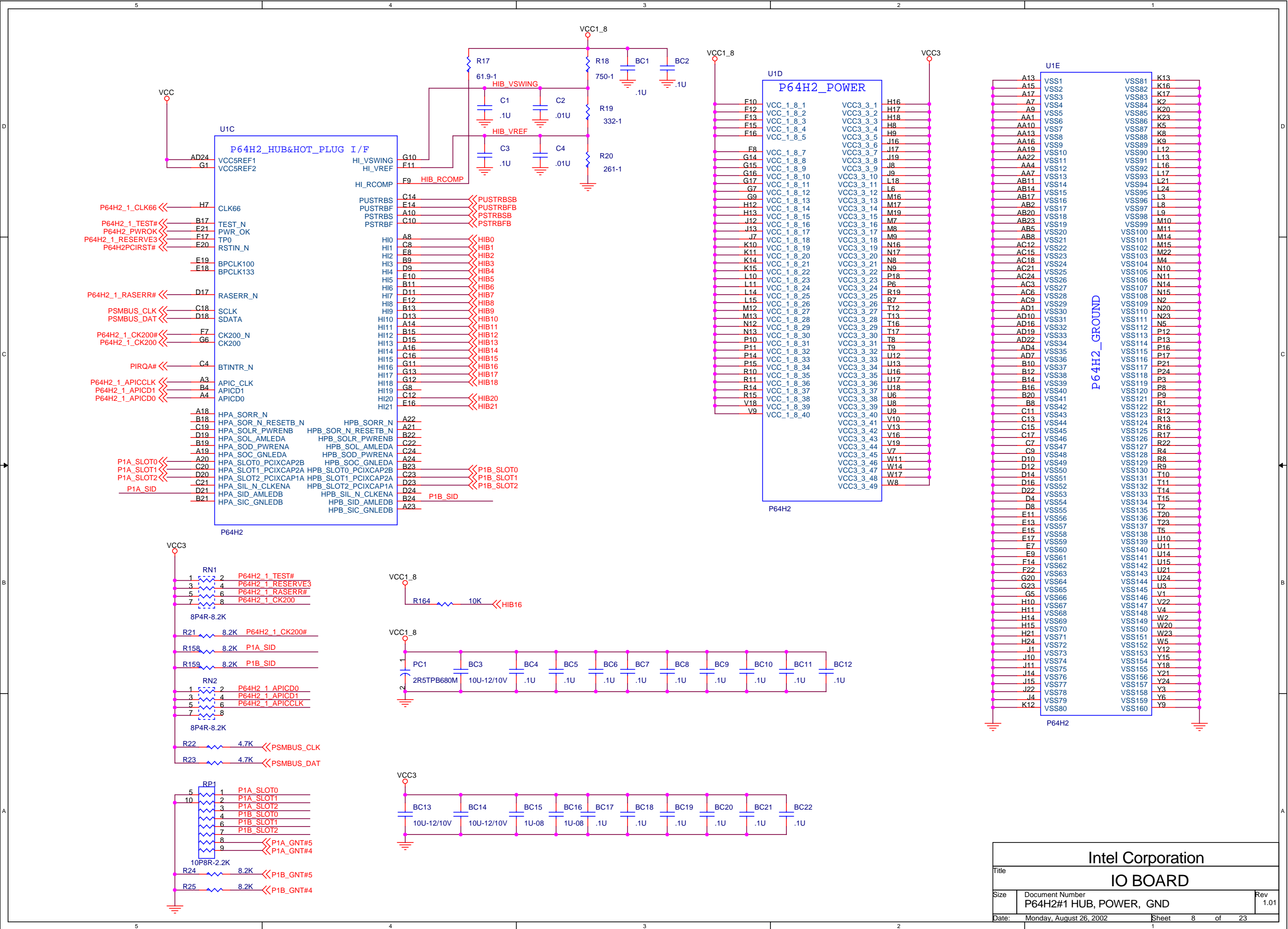
JUMPERS:

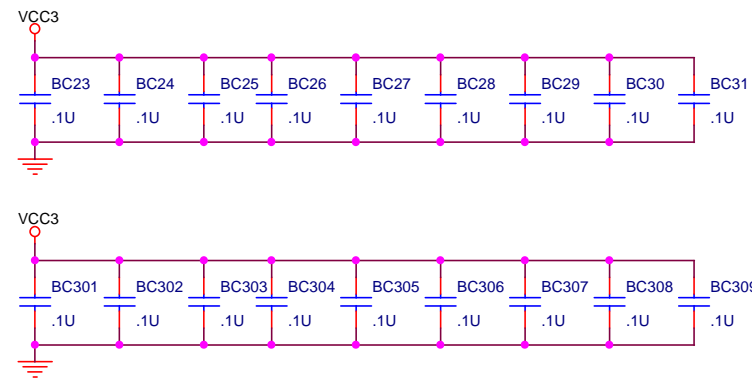
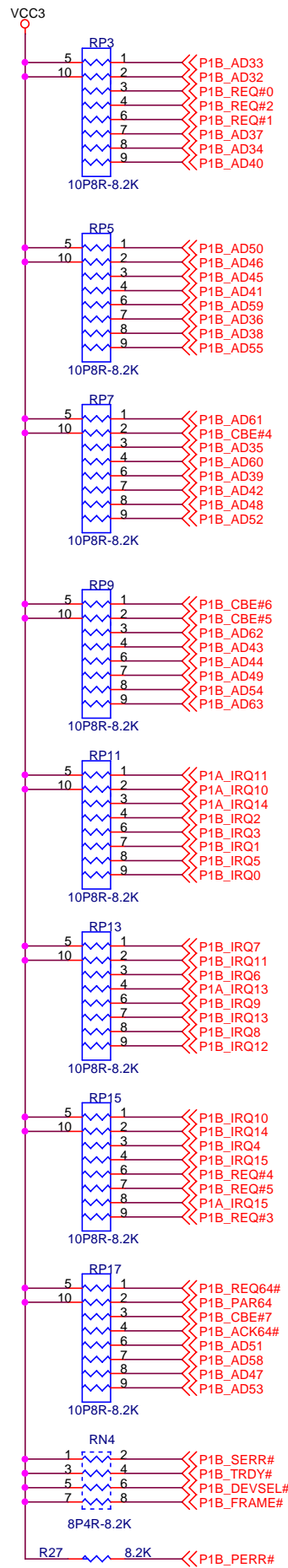
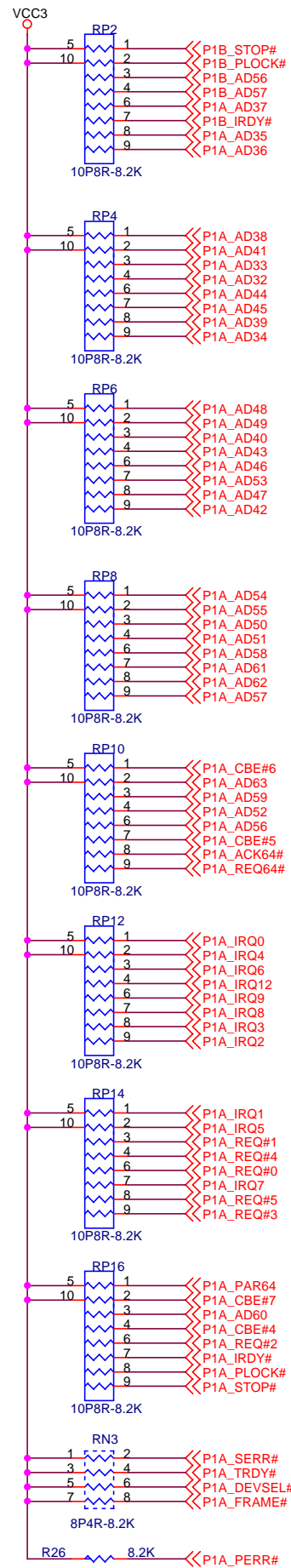
JP1: DP/UP SELECTION FOR ITP PORT
1-2 DP DEFAULT
2-3 UP
JP2: CPU SAFE MODE
ON ENABLE DEFAULT
OFF DISABLE
JP3: CLEAR CMOS
1-2 NORMAL DEFAULT
2-3 CLEAR CMOS
JP4: ICH3 TCO TIMER
ON DISABLE
OFF ENABLE DEFAULT
JP5: VRM ID SELECTION
JP6: CPU FAN POWER
1-2 +12V
2-3 5V

P64H2#3:
P3AIRQ0: PCI-X SLOT
P3AIRQ1: PCI-X SLOT
P3AIRQ2: PCI-X SLOT
P3AIRQ3: PCI-X SLOT

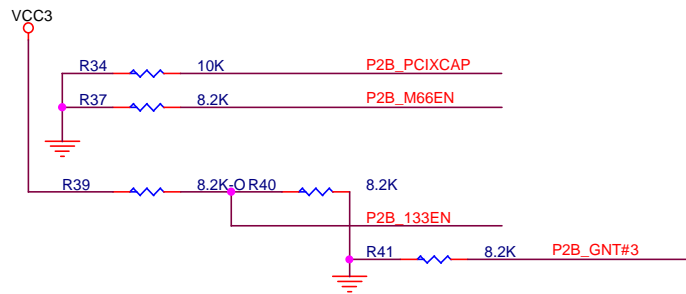
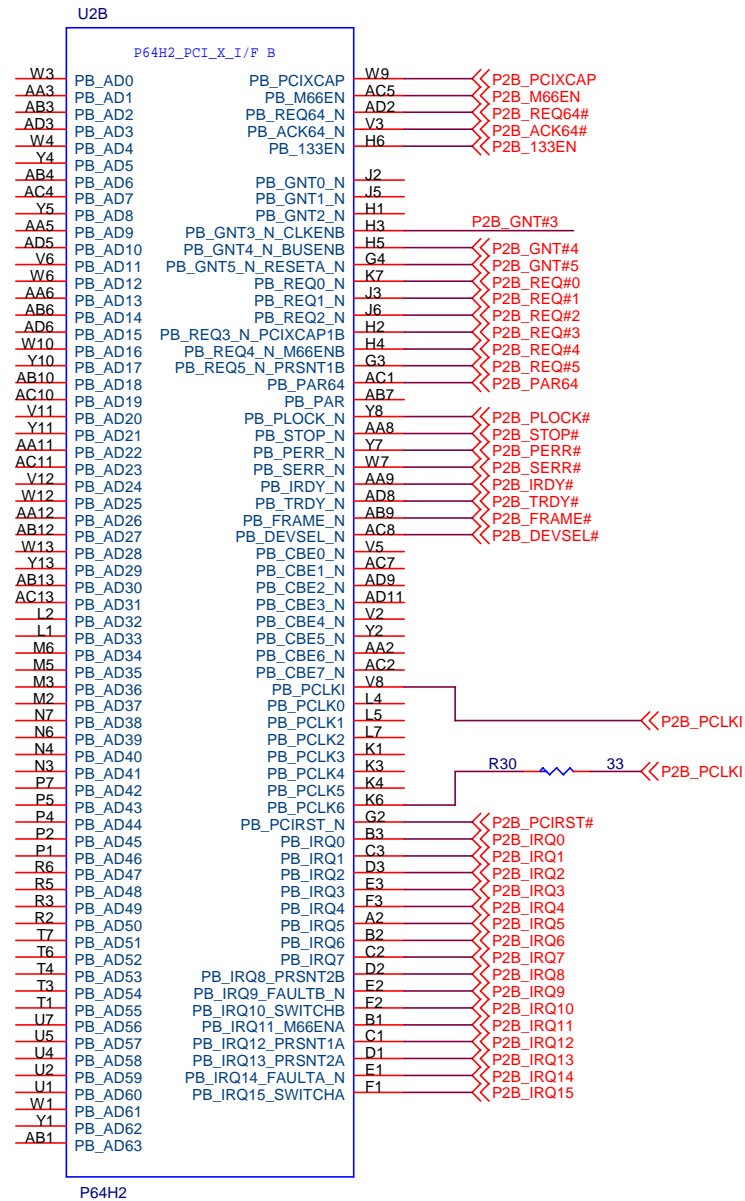
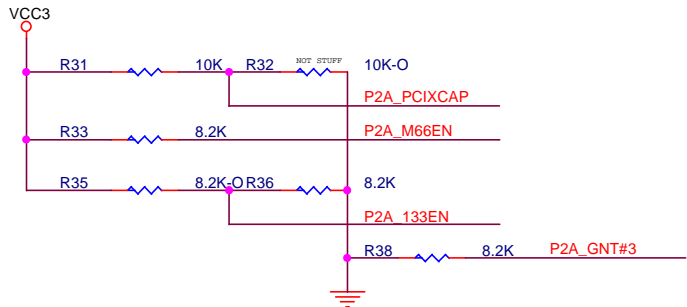
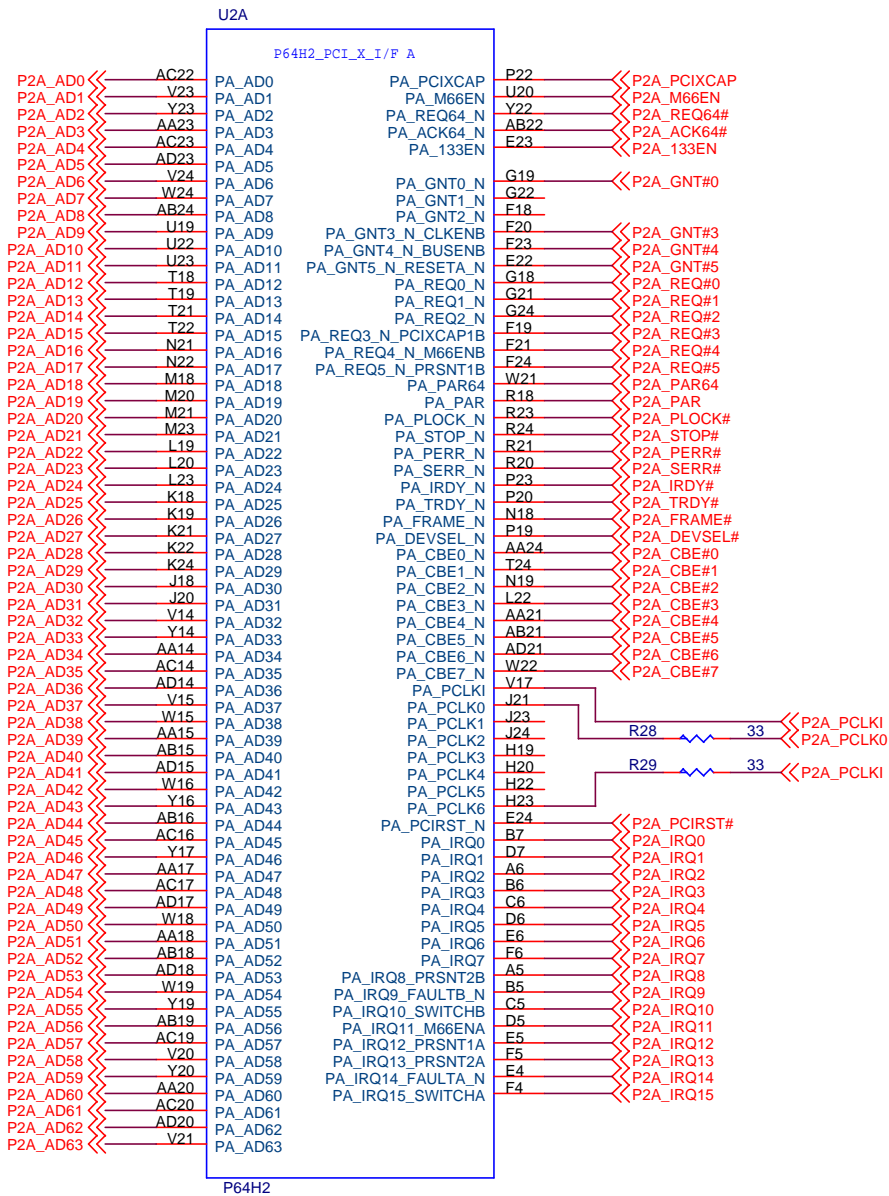


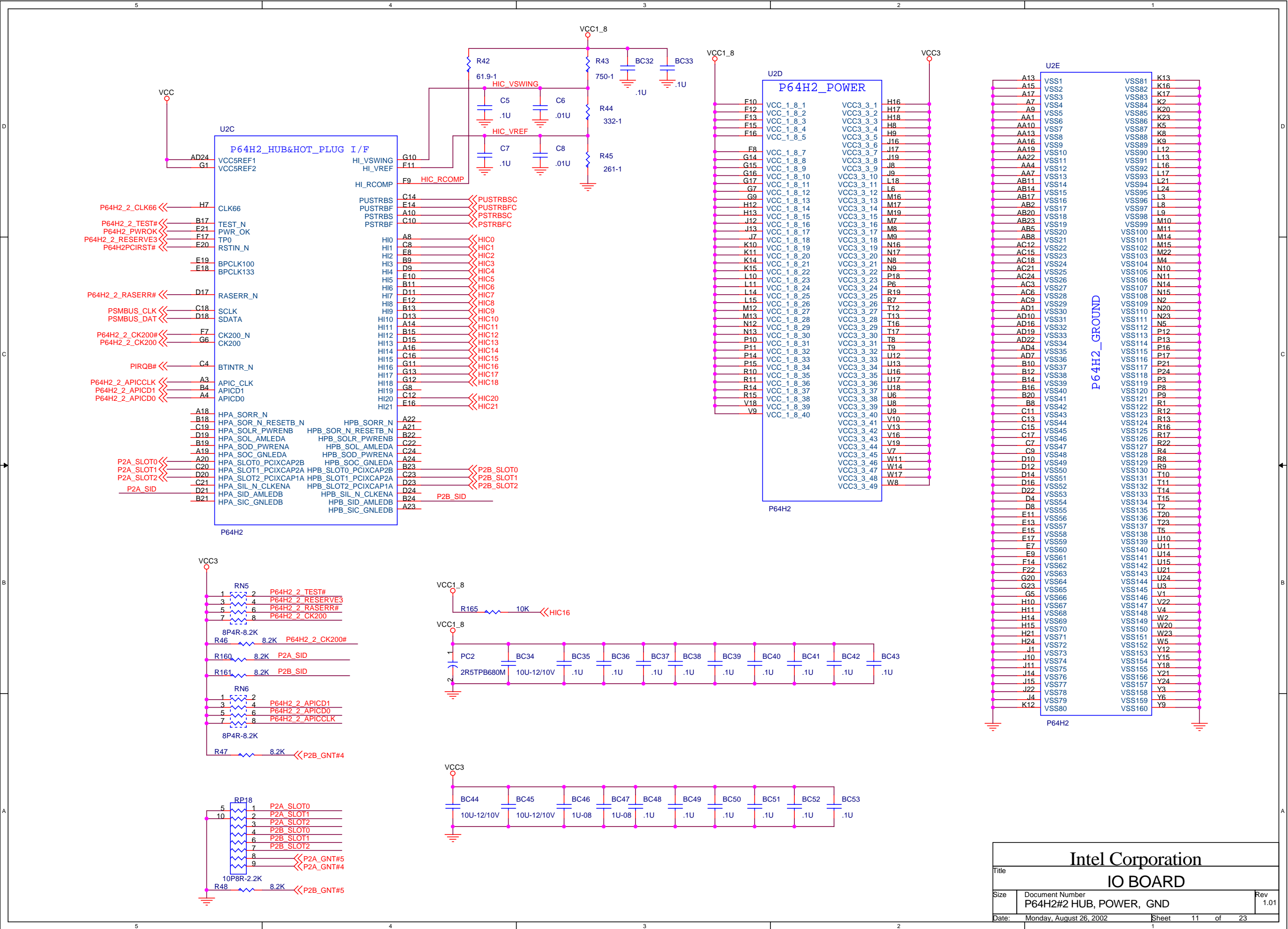
Intel Corporation			
Title			
IO BOARD			
Size	Document Number	Rev	1.01
P64H2#1 PCI-X BUS A, B			
Date:	Monday, August 26, 2002	Sheet	7 of 23

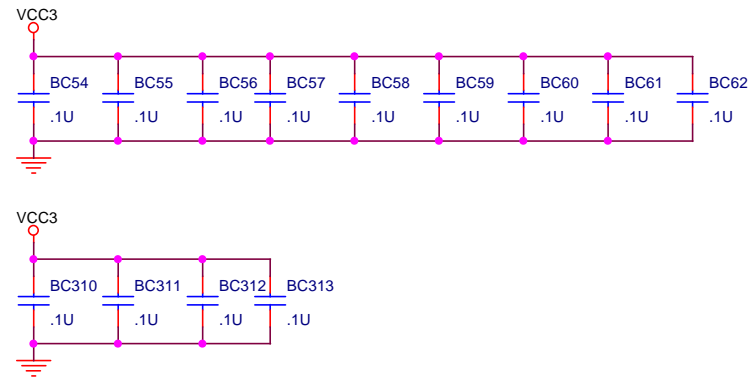
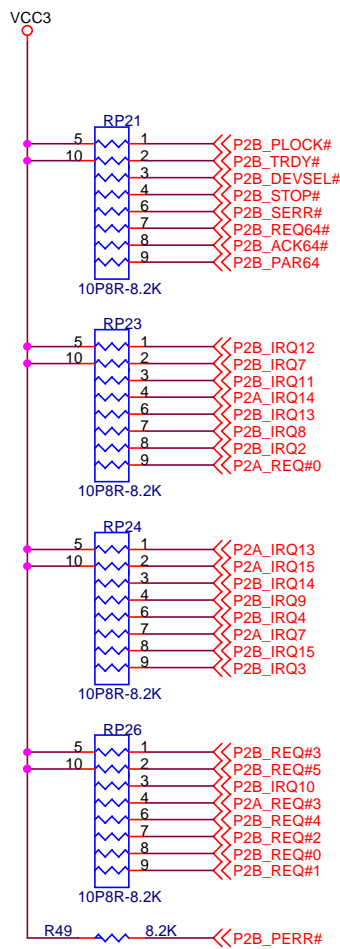
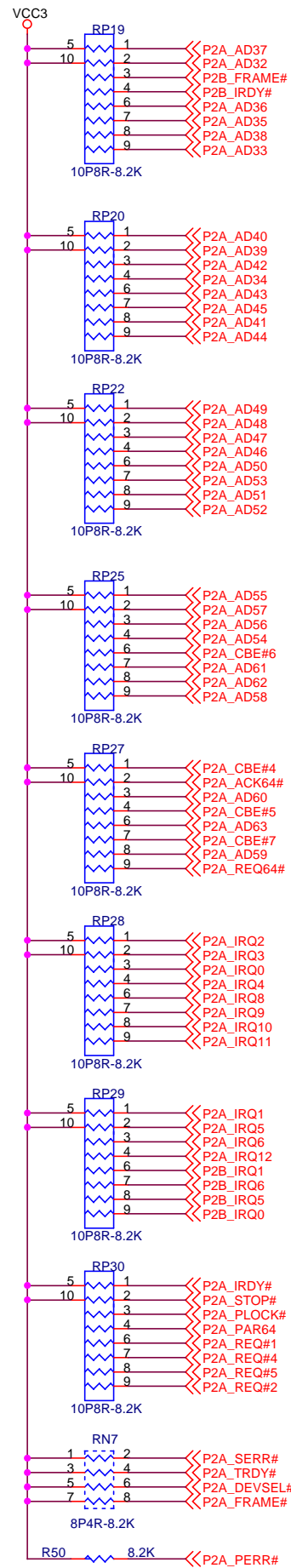


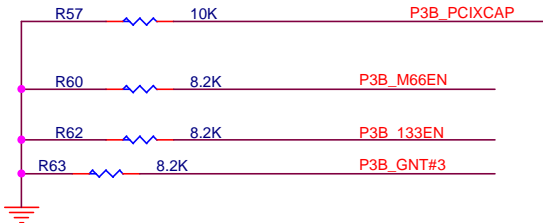
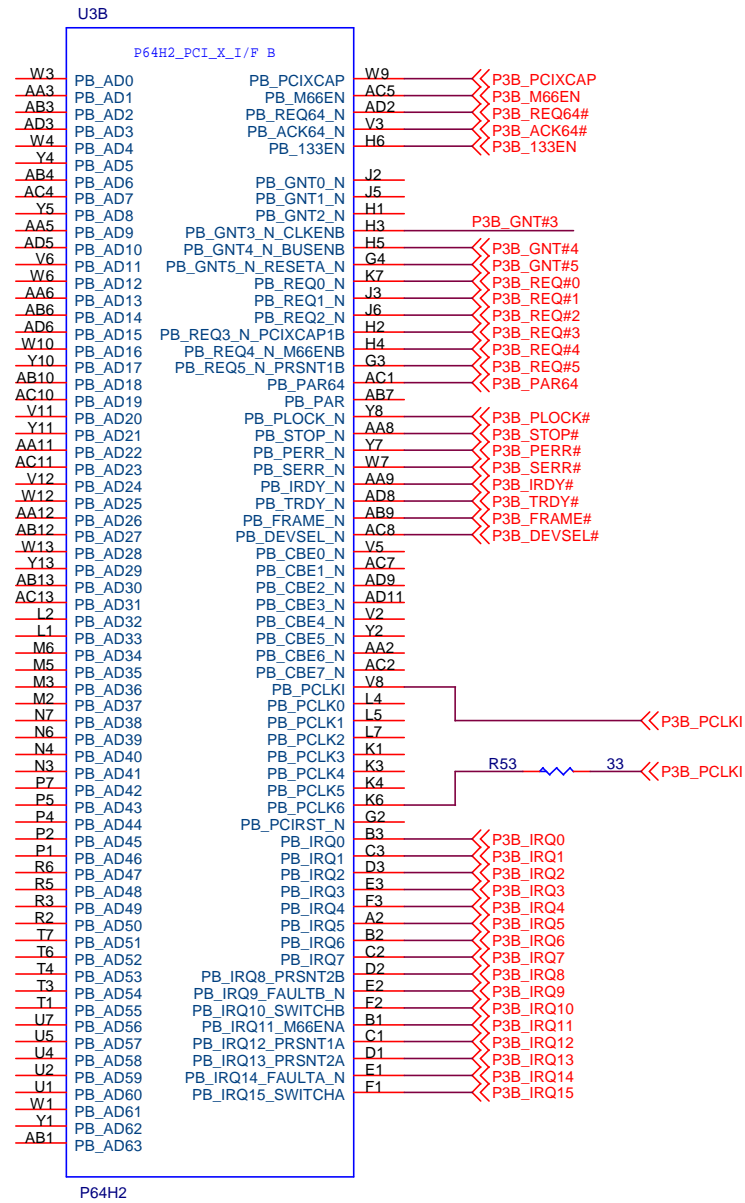
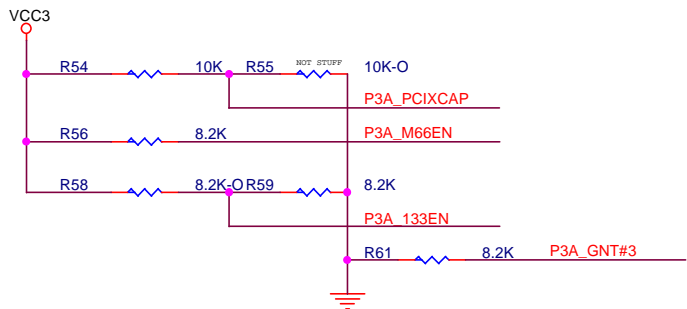
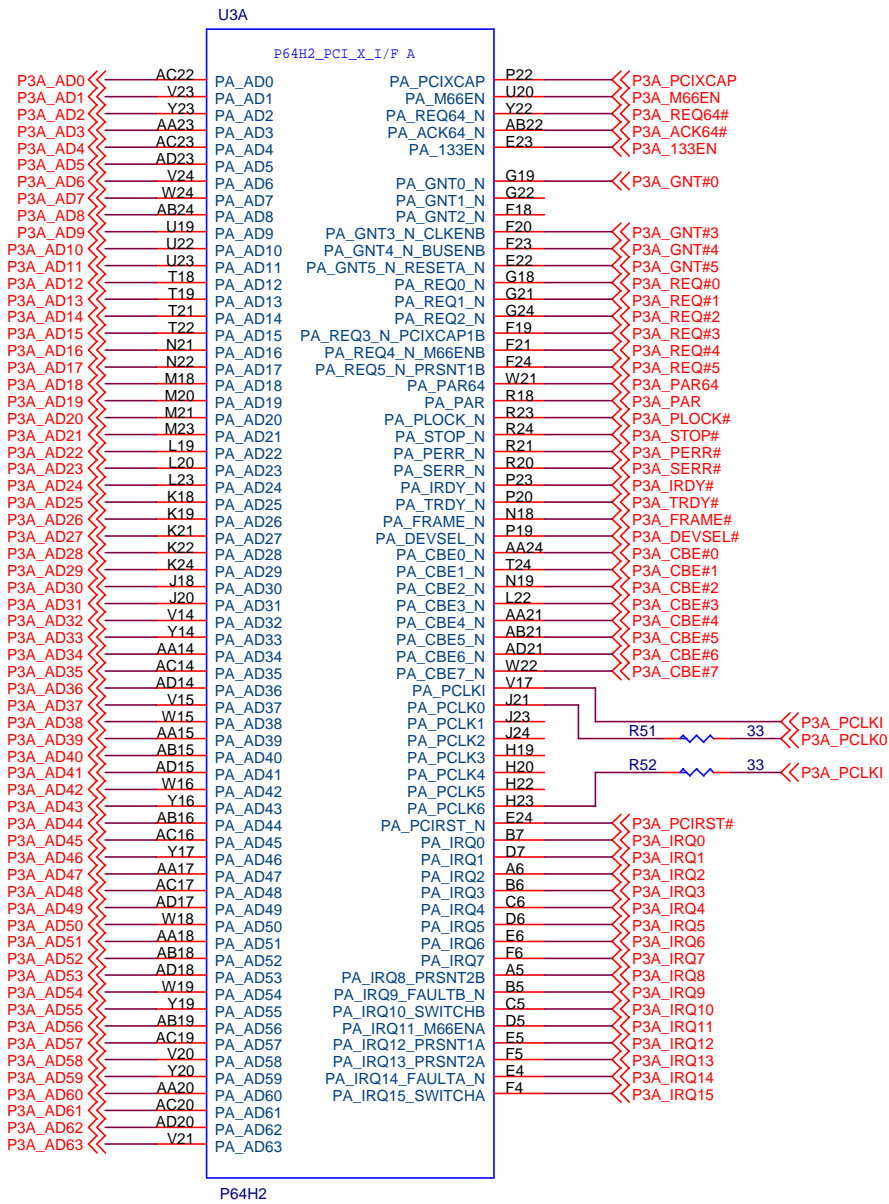


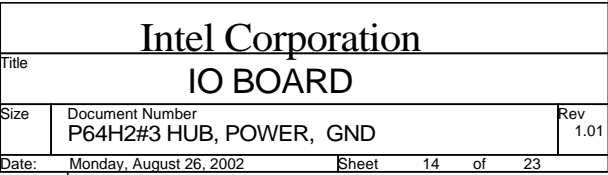
Intel Corporation			
IO BOARD			
Title	P64H2#1 TERMINATORS		
Size	Document Number	Rev	1.01
Date:	Monday, August 26, 2002	Sheet	9 of 23

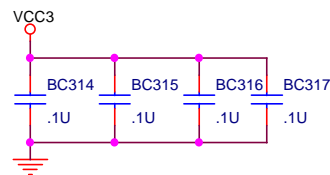
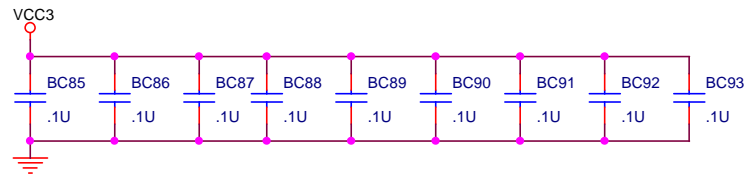
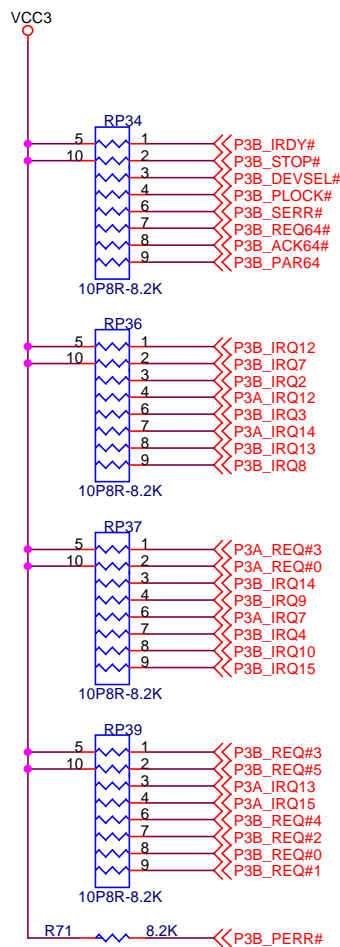
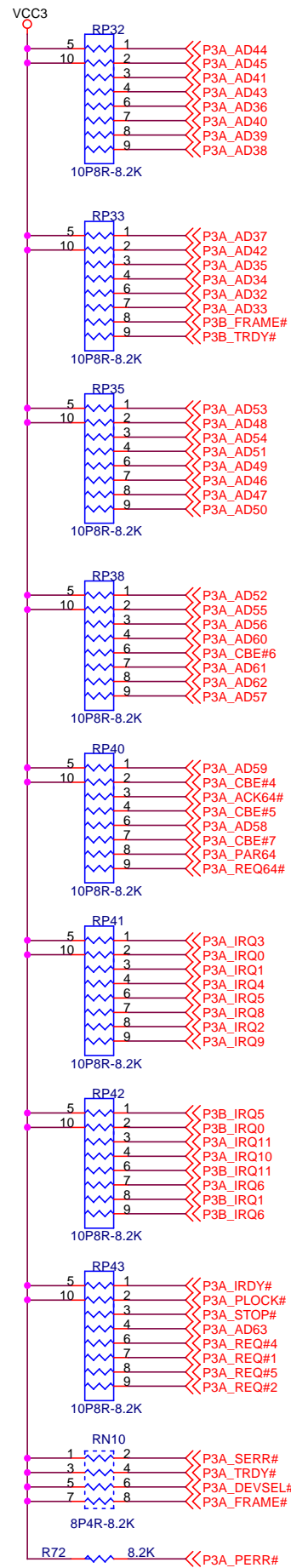












Intel Corporation

IO BOARD

Title		
P64H2#3 TERMINATORS		
Size	Document Number	Rev
		1.01
Date:	Monday, August 26, 2002	Sheet 15 of 23

